

Claims

- [c1] What is claimed is:
- 1.A method for determining interface traps in a semiconductor/oxide interface of a MOS transistor comprising a bulk substrate, a source, a drain, a gate, and a silicon oxide layer beneath the gate, the method comprising:
- grounding the bulk substrate, source, and drain;
- applying a first gate pulse having a fixed low-level gate voltage (V_{gl}) and an increasing high-level gate voltage (V_{gh}) at a high gate pulse frequency on the gate so as to obtain a first charge-pumping current (I_{CP})- V_{gh} curve;
- applying a second gate pulse having same low-level gate voltage (V_{gl}) and same increasing high-level gate voltage (V_{gh}) as the first gate pulse at a low gate pulse frequency on the gate so as to obtain a second I_{CP} - V_{gh} curve; and
- subtracting the second I_{CP} - V_{gh} curve from the first I_{CP} - V_{gh} curve.
- [c2] 2.The method of claim 1 wherein the second I_{CP} - V_{gh} curve is approximately equal to a leakage current component.
- [c3] 3.The method of claim 1 wherein the silicon oxide layer has a thickness of less than 30 angstroms.
- [c4] 4.The method of claim 1 wherein the silicon oxide layer has a thickness that is in a direct tunneling regime.
- [c5] 5.The method of claim 1 wherein the high gate pulse frequency is about 1 MHz and the low gate pulse frequency is about 10^4 to 10^5 Hz.
- [c6] 6.A method for testing a MOS transistor having an ultra-thin gate oxide layer, wherein the MOS transistor comprises a bulk substrate, a source, a drain, a gate, and an ultra-thin gate oxide layer disposed between the gate and the bulk substrate, the method comprising:
- grounding the bulk substrate, source, and drain, wherein the source and the drain are electrically connected to each other;
- applying a first gate pulse having a fixed low-level gate voltage (V_{gl}) and an increasing high-level gate voltage (V_{gh}) at a high gate pulse frequency on the gate so as to obtain a first I_{CP} - V_{gh} curve;

applying a second gate pulse having same low-level gate voltage (V_{gl}) and same increasing high-level gate voltage (V_{gh}) as the first gate pulse at a low gate pulse frequency on the gate so as to obtain a second $I_{CP} - V_{gh}$ curve; and subtracting the second $I_{CP} - V_{gh}$ curve from the first $I_{CP} - V_{gh}$ curve so as to obtain a third $I_{CP} - V_{gh}$ curve that is regarded as a real charge-pumping current curve at the low gate pulse frequency.

[c7] 7.The method of claim 6 wherein the ultra-thin gate oxide layer has a thickness of less than 20 angstroms.

[c8] 8.The method of claim 6 wherein the ultra-thin gate oxide layer has a thickness that is in a direct tunneling regime.

2013-06-03 10:40:40